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WILLKIE FARR & GALLAGHER LLP
INTELLECTUAL PROPERTY LEGAL ASSISTANTS
787 SEVENTH AVE
NEW YORK, NY 10019-6099

EXAMINER	
NGUYEN BA, HOANG VU A	
ART UNIT	**PAPER NUMBER**
2192	

DATE MAILED: 07/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/434,394	YATES ET AL.	
	Examiner	Art Unit	
	Hoang-Vu A. Nguyen-Ba	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59 and 61-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,40-59 and 61-65* is/are allowed.

6)☒ Claim(s) *2,9,10,12-14,19-22 and 30* is/are rejected.

7)☒ Claim(s) *3-8,11,15-18,23-29 and 31-39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/31/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the amendment filed March 31, 2006.

2. Claims 1-59 and 61-65 remain pending.

Information Disclosure Statement

3. The Office acknowledges receipt of the Information Disclosure Statement dated March 28, 2006. It has been placed in the application file and the information referred to therein has been considered.

Response to Arguments

4. Applicants' arguments with respect to Claims 1-59 and 61-65 have been considered but they are not persuasive. The following is an examiner's response to Applicants' arguments.

I. Paragraph 20: Claims 2, 9, 12 and 14 and Patentable Over Takusagawa

A. "Segment descriptor"

Applicants argued that the Office action does not designate any particular element of Takusagawa to correspond to the "segment descriptor" of claim 2 and without such a designation or explanation of pertinence, it is difficult to interpret the Office action.

In response to this argument, it is noted that relevant portions of Takusagawa have been cited in the Office action (e.g., 2:40-43, 50-62, 4:36-38) to support the rationale for the rejection of the claimed features as being anticipated by Takusagawa. According to these cited passages

of Takusagawa, the claimed "segment descriptor" appears to read on Takusagawa's "valid field" 212 and "clean field" 213.

It is further noted that applicants fail to clearly define the claimed "segment descriptor" either in the claim or in the description. Thus, the segment descriptor is broadly and reasonably interpreted to be a field in a data structure that contains a bit indicating the status of a device. This interpretation is not considered unreasonable in view of the definition of the term of art "Segment Descriptor" in Applicants' submitted Exhibit A (see page 3-9, last paragraph; "A segment descriptor is a data structure ... that provides the processor with ... as well as ... status information."). It is also noted that since applicants do not clearly specify the scope of the term segment descriptor either in the claim or in the specification, the limitation "segment descriptor" must be given the broadest reasonable interpretation without unnecessarily including all the limitations shown in FIG. 3-8 of Exhibit A and which are not relevant to the invention claimed in this instant application. Thus, Applicants' argument that the definition of the term of art distinguishes over Takusagawa's "valid register" 102, "valid register" 202, "valid register" 302, "valid field" 212, and "clean field" 213 (see FIG. 1) is unpersuasive.

Applicants further argued that "Segment descriptor" is a term of art (Exhibits A and B) and that Takusagawa' s store-in cache is not a "segment descriptor." Moreover, Applicants submitted that because "segment descriptor" is a term of art that distinguishes the TLB discussed in Cmelik '992 and Cmelik's TLB is similar to Takusagawa' store-in cache, it is difficult to discern the view expressed in the Office action.

In response to these arguments, it is respectfully noted that:

i) the "Segment descriptor" appears to be not a **term of art** as asserted by Applicants. There seems to be no entry such as "segment descriptor" either in the Authoritative Dictionary of IEEE Standards Terms, Seventh Edition or in the Microsoft Press Computer Dictionary, Third Edition, copies of relevant pages being attached herewith.

ii) Applicants appear to have misconstrued the relevance of the cited portions of Takusagawa. The claimed "segment descriptor" is not interpreted by the Office action to be equivalent to the alleged "store-in cache." Rather, it is more reasonable to interpret the claimed "segment descriptor" to read on Takusagawa's "valid register" 102, "valid register" 202, "valid register" 302, "valid field" 212 and "clean filed" 213, as discussed previously.

B. "Well-behaved Memory"

Applicants argued that Paragraph 20 of the Office action does not designate anything in Takusagawa '484 as corresponding to the "device having a valid memory address but that cannot be guaranteed to be well-behaved."

In response to this argument, it is noted that the claimed "device," "a valid memory address," "but that cannot be guaranteed to be well-behaved" are interpreted to read on Takusagawa's "store-in cache," "address array having valid memory address indicated by a 1 in the valid

field" and "address array having memory address indicated by a 0, i.e., incoincident, in the clean filed," respectively.

Applicants further argued that "well-behaved memory" issue was resolved to the examiner's satisfaction by Applicants' explanation of the term at pages 16-17 of the Response of August 4, 2004 and in Applicants' originally filed specification. Applicants further submitted that "well-behaved memory" is different than whether "a fault is detected."

Responsive to the above arguments, the Office action indeed interpreted the limitation "well-behaved memory" in light of applicants' specification, which is memory from which [an issued] load [instruction] will receive the data last stored at the memory location. In Takusagawa (2:40-44), among other things, the valid field 212 of the address array represents whether the entry is valid (e.g., V=1 when valid) and when the entry is valid whether the content of the entry is coincident (C=1, clean) with the content of the main memory (i.e., the specified "data last stored at the memory location"). If these two conditions (i.e., valid and coincident) are met, there is a cache hit (or the claimed "well-behaved memory"). The Office action (¶ 20, Claim 2 rejection) does not appear to equate "Well-behaved memory" with "whether a fault is detected" in the 102(a) rejection, as alleged by Applicants' representative.

C. Conclusion: Claims 2, 9, 12 and 14 are Patentable Over Takusagawa '484

Applicants submitted that for reasons discussed in ¶¶ I.A and I.B of Applicants Response, claim 2 is patentable over Takusagawa '484, and

Applicants submitted that for reasons discussed in ¶¶ I.A and I.B of Applicants Response, claim 2 is patentable over Takusagawa '484, and the Office action is too incomplete procedurally to raise any rejection over Takusagawa '484.

In response, it is respectfully noted that had Applicants' representative fully considered the evidence contained in the portions of Takusagawa cited in the previous Office action to support the rejection of claim 2 as being anticipated by Takusagawa, Applicants would have easily understood that the features recited in claim 2 read on Takusagawa teachings. Therefore, Applicants' argument that the Office action is too incomplete procedurally to raise any rejection over Takusagawa merely amounts to a general allegation without any specific support for this rationale. For Applicants' representative's convenience, the Office action has provided in the foregoing discussion more detailed explanation of the relevancy of Takusagawa, thereby fully addressing Applicants' concerns. The rejection of claim 2 under 102(a) as being anticipated by Takusagawa is thus considered proper and maintained.

With respect to claim 14, which recites similar language of claim 2, the rejection is maintained for the same reasons.

With respect to claim 9, Applicants appear to argue that Takusagawa does not disclose that his store-in cache memory is a "device having a valid memory address... in an I/O space of a computer." Applicants further submitted that "[i]f any rejection is thought to apply, Applicants requests a specific designation of the "address" of the component, and of the "I/O space."

In response to arguments regarding claim 9, it is noted that in FIG. 1, there are shown a "Processor," "Main Memory," and between these two components the pipelined structure of the store-in cache memory. First, in order for the processor to issue a request for accessing the main memory, the processor has to know where to send the request or alternatively stated, the store-in cache memory has to have a valid address so that the processor knows where to send the request. Second, since the store-in cache memory is neither part of the main memory nor part of the processor, it has to be in the Input/Output part of the computer, part where data are prepared for processing by the processor and the results are either stored in the main memory of the computer or outputting to a peripheral device. Therefore, the claimed feature "the device having a valid memory address has an address in an I/O space of the computer" is deemed illustrated in FIG. I of Takusagawa, as pointed out by the previous Office action.

With respect to claim 12, Applicants argued that the "segment register" is a term of art shown in Exhibits A and B and that a "valid register" in a write-in cache is not a "segment register."

Since the term "segment register" is not specifically defined in the Applicants' specification or claim, and that "segment register" seems to be not a term of art, as asserted by Applicants, because there appears to be no entry corresponding to a "segment register" either the Authoritative Dictionary of IEEE Standards Terms, Seventh Edition or in the Microsoft Press Computer Dictionary, Third Edition, copies of relevant pages being attached herewith. According to the cited Reference Dictionaries, Takusagawa's "valid register" appears to read on

the claimed segment register which is interpreted to be a register with a segment or data (i.e., "valid" bit). It is further noted that limitations in Exhibits A and B should not be read unnecessarily into the claim.

II. Paragraph 12: Claim 3 is Patentably Distinct from Claim 7 of the '379 Patent

Applicants submitted that the Office action is rather confusing: the view stated in this Office action are inconsistent with views stated in earlier Office action.

In response, it is not understood why the Office action is confusing and inconsistent since the above-mentioned Office actions contain different grounds of rejection, thus different views.

First, Applicants argued that the Office action misidentifies the differences between the claims and only addresses some of the differences. Applicants further argued that without a consideration of all the differences, it is difficult to respond directly.

In response to the first argument, it is noted that the Office action has identified all the differences between the claims and shown that these discrepancies appear to have been cured by the teaching of Takusagawa.

Regarding the underlined portions of the claims that are not shown in the Office actions but shown in Applicants response:

i. based at least in part on an annotation encoded in a segment descriptor: this limitation is deemed inherent in the process of evaluating whether an individual memory reference of an instruction references a device having a valid memory address but that cannot be guaranteed to be

well-behaved. In order for such an evaluating process to be operative, there should be a field in the data structure that indicates that the address is valid and another field of the data structure that indicate that the device is not guaranteed to be well-behaved. Without these annotations encoded in the segment descriptor, the evaluating process would be inoperative. In fact, these annotations are indeed present in Takusagawa teachings: a valid address is indicated by the valid bit, well-behaved memory is indicated by an invalid bit in the first register when no fault is detected; and a not well-behaved memory by an invalid bit in a third register.

ii. evaluating whether an individual memory reference of an instruction references a device that cannot be guaranteed to be well-behaved: Applicants' attention is respectfully directed to the claim language of instant claim 2, which is apparently **similar** to that of patent claim 7. It is not clearly understood the differences, as pointed out by Applicants, between the instant claims and the patent claims as far as this step is concerned.

Second, Applicants argued that it was previously acknowledged that "an annotation encoded in a segment descriptor" is a non-obvious difference in view of Applicants arguments in previous responses (see Applicants' Remarks, page 5). Applicants further submitted that until an Office action "answers all material traversed" as required by MPEP § 707.07(f) and states a view on this issue, the 12/28/05 Office action is

procedurally insufficient to raise any rejection and Applicants requested that "annotation encoded in a segment descriptor" language of the claims be considered.

In response to the last argument, the Office respectfully directs Applicants' attention to the aforementioned discussion of segment descriptor and in ¶ I.A. Accordingly, the view of the Office is that the limitation "annotation encoded in a segment descriptor" is not a patentably distinct subject matter over patent '379 because this feature is not a novelty in the art and is obvious over Patent claim in view of Takusagawa teachings.

Third, Applicants argued that the Office action equates determining whether memory is "well-behaved" with whether a fault is detected; that the Office action does not suggest that Takusagawa '484 determines whether memory is "well-behaved"; and that this is a non-obvious difference between the claims.

In response to the first statement of Applicants' third argument, the Office notes that the statement reflects one of the reasonable interpretations of the limitation "well-behaved" in light of the definition of the term in the specification. "Well-behaved" is defined to be the behavior of a memory which receives data last stored at a memory location as a result of a load instruction. Takusagawa teaches a similar condition when no fault is detected, i.e., when the data stored in the cache memory is similar to the data stored in the main memory ("cache hit" condition).

In response to the second statement, Applicants' attention is directed to the previous Office action, page 7, second ¶.

In response to the third statement, the "well-behaved" limitation is not considered to be a non-obvious feature between the claims in view of the rationale expressed in the Office action page 7, second ¶ and repeated hereinabove.

Fourth, Applicants argued that the Office action picks and chooses bits and pieces of Takusagawa '484 for piecemeal substitution into the '379 claims. The Office action is simply silent on the interrelationships recited in the claims – it makes no showing that it would be obvious to combine the '379 claims plus bits and pieces of Takusagawa '484, to obtain the interconnections recited in claims 2+3.

In response to Applicants' fourth argument, the Office notes that: first, the bits and pieces in Takusagawa are all parts of an embodiment (claim 7+8+9+10+11+12), thus, they are interrelated and must be considered as a whole; second, the motivation to combine the teachings of Takusagawa with Patent '379 is the common objective making appropriate corrections (e.g., re-executing the instructions in an alternative execution mode – Patent claim 7) to improve system reliability and performance.

Fifth, Applicants argued that the Office action relies on Takusagawa '484, col. 1, lines 39-42 for "motivation to combine." This motivation to modify or combine is for a store-in cache memory which is not related to the subject matter of the '379 claims. Therefore, Applicants submitted that "[n]o double patenting rejection is raised, and none is warranted."

In response to Applicants' fifth argument, the Office interprets that Applicants' argument infers that Takusagawa is nonanalogous art, therefore the cited motivation to combine is improper. It has been held that a prior art reference must either be in the field of Applicants' endeavor or, if not, then be reasonably pertinent to the particular problem with which Applicants were concerned, in order to relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir.1992). In this case, Takusagawa is concerned with fault detection and correction in cache memory for the purpose of improving processing performance and system reliability (1:39-42). And the instant invention is related to determination of well-behaved and non well-behaved for the purpose of determining which program transformation optimizations are safe and correct and which present a risk of error (instant specification, p. 27, 2nd ¶). Thus, both inventions are in the analogous art and try to reach the same goal of system optimization and reliability.

III. Paragraph 15: Claims 22 and 30 Are Patentably Distinct From Claims 8 of the '379 Patent

Applicants essentially argued that: paragraphs 14 and 15 of the Office action do not purport to reject either claim 22 or 30; no rejection exists; nonetheless, in a good faith effort to advance prosecution, Applicants note:

a. Paragraphs 14 and 16 of the Office action are silent on the language "segment descriptor" that has been noted in Applicants' two previous papers. A prior Office action conceded that "segment descriptor" is a non-obvious difference over the prior art. See discussion item "Second" at page 5, above.

In response to Applicants' argument that ¶¶s 14 and 16 of the Office action are silent on the language "segment descriptor," the Office notes that the Office action has cited the relevant portion of Takusagawa (i.e., 2:40-43) that is considered to read on not only the limitation "segment descriptor" (see also discussion in ¶ I.A. and item "Second") but that of "based at least in part on an annotation encoded in a segment descriptor." Therefore, the previous Office action is not silent on the language "segment descriptor," as alleged by Applicants.

In response to Applicants' argument that a prior Office action conceded that "segment descriptor" is non-obvious difference over the prior art, it is respectfully noted that "non-obvious difference" is clearly different from "difference." The Office action did not assert that there is a "non-obvious difference" (see prior Office action, page 8, 2nd, 3rd and 4th ¶¶s). Instead, the Office action submitted that:

'379 Patent Claims 4+8 contain every element of instant Claim 22 except the limitation "based at least in part on an annotation encoded in a segment descriptor," "aborting the identified memory load," and "based at least in part on the identifying;"

However, these differences are taught by Takusagawa (see prior Office action, page 8, 3rd ¶). Therefore, It would have been obvious to a person of ordinary skill in the art at the time the invention was made to add these steps taught by Takusagawa to the '379 Patent teachings as this would provide the '379 Patent

teachings with necessary information to determine whether a memory is well-behaved or not well-behaved for the purpose of making appropriate corrections to improve system reliability and performances.

Therefore, it is submitted that the Office action never conceded that "segment descriptor" is a non-obvious difference over the prior art and there is an **obvious** difference over the Patent claims rather than a **non-obvious** difference, as alleged by Applicants.

b. Applicants argued that the "'379 teachings" (Office action of 12/28/05 at page 8, lines 17-18 and page 9, line 14-15) may not be relied upon. MPEP § 804(B)(1) ("the disclosure of the patent may not be used as prior art.").

In response to the above argument, it is respectfully noted that MPEP § 804(B)(1) also indicates that although "the disclosure of the patent may not be used as prior art... This does not mean that one is precluded from all use of the patent disclosure... The specification can be used as a dictionary to learn the meaning of a term in the patent claim... Further, these portions of the specification which provide support for the patent claims may also be examined and considered when addressing the issue of whether a claim in the application defines an obvious variation of an invention claimed in the patent... The court in *Vogel* recognized "that it is most difficult, if not meaningless, to try to say what is or is not an obvious variation of a claim," but that one can judge whether or not the invention claimed in an

application is an obvious variation of an embodiment disclosed in the patent which provides support for the patent claim. According to the court, one must first "determine how much of the patent disclosure pertains to the invention claimed in the patent" because only "[t]his portion of the specification supports the patent claims and may be considered." The court pointed out that "this use of the disclosure is not in contravention of the cases forbidding its use as prior art, nor is it applying the patent as a reference under 35 U.S.C. § 103, since only the disclosure of the invention claimed in the patent may be examined." In this case, although pertinent claims in Takusagawa that define the obvious variation of the invention claimed in instant claim 22 are not specifically mentioned in the previous Office action, the disclosure of these claims are nonetheless cited to provide proper support for the obviousness-type double-patenting rejection of claim 22 over patent claims 4+8 in view of Takusagawa's portions of the disclosure that define claims that recite an obvious variation of the invention claimed by instant claim 22.

c. Applicants argued that "[t]he motivation to combine" stated in the Office action is incorrect. See discussion item "Fifth" at page 6, above."

In response to the argument, the Office respectfully directs Applicants' attention to the response to the "fifth" argument above.

Applicants further argued that prosecution cannot advance when several successive Office actions have been silent on the same issue.

In response, the Office notes that it has made an best effort to appropriately address the issued raised by Applicants and requests Applicants do the same to advance prosecution of this application, thereby optimizing time and resources of Applicants and the USPTO.

IV. Paragraph 8: Claim 14 is Not a "single Means Claim"

Applicants argued that MPEP § 2164.08(c) states that a "single means claim" can only exist where a claim recites a "means" element, that claim 14 recites no "means" element, that it is a "zero means" claim, and no rejection is warranted.

As an initial matter, responsive to the above argument, the Office respectfully notes that MPEP 2164.08(c) refers to "Critical Feature Not Claimed" rather than "Single Means Claim." Applicants' argument is thus moot. Nonetheless, in a good faith effort to advance prosecution, the Office notes the following:

MPEP 2164(a) says "... When claims (e.g., claim 14) depend on a recited property (e.g., ...evaluate, based at least in part on an annotation encoded in a segment descriptor, whether an individual memory-reference instruction, ... references a device with a valid memory address that cannot be guaranteed to be well-behaved), a fact **comparable** (emphasis added; note that MPEP does not say "identical"; in case "identical" is indicated, the claim language must recite "means for" in order to justify the reliance on *Hyatt*) *Hyatt* is possible, where the claim covers every conceivable structure (means) for achieving the stated property (result) while the specification discloses at most only those known to the inventor."

Since an instruction execution circuitry is merely a structure or means and claim 14 recites only **one** circuitry, claim 14 is thus a "single means claim."

The rejection of claim 14 under 35 U.S.C. § 112, first paragraph, as being a single means claim is considered proper and maintained.

V. Paragraphs 9, 10, 11- Claims 2 and 14 are "Complete" As Required by Law

Applicants argued the following:

claims 2 and 14 were drafted in reliance on PTO policy as set forth in MPEP § 2172.01;

all elements of claims 2 and 4 are interconnected; none have a "gap between" them; to raise a rejection based on § 2172.01, and Office action must identify two elements that are in the claim, and show that there is no interconnection; the Office action fails to mention any relevant facts that might support a rejection.

In response to the above two arguments, the Office notes that MPEP § 2172.01, 2nd ¶ indicates that:

> In addition, a claim which fails to interrelate essential elements of the invention as defined by applicant(s) in the specification may be rejected under 35 U.S.C. § 112, second paragraph, for failure to point out and distinctly claim the invention

Furthermore, MPEP § 2173 discusses the requirements of claims that must particularly point out and distinctly claim the invention as follows:

> The primary purpose of this requirement of definiteness of claim language is to ensure that the scope of the claims is clear so the public is informed of the boundaries of what constitutes infringement of the patent. A second purpose is to provide a clear measure of what applicants regard as the invention so that it can be determined whether the claimed invention meets all the criteria for patentability and whether the specification meets the criteria of 35 U.S.C. § 112, first paragraph with respect to the claimed invention.

In the instant application, claim 2, with only one step (i.e., the step of evaluating whether an individual memory reference of an instruction references a device...), does not particularly point out and distinctly claim the invention so that the scope of claim 2 is sufficiently clear so that the public is informed of the boundaries of what constitutes infringement of the patent. In view of this rationale, it would appear that instant claim 2 infringes the Takusagawa patent.

The Office agrees with Applicants that it cannot identify two steps that are in the claim and show that there is interconnection as argued by Applicants because Claim 2 has only one step. Claim 2 has to have at least one additional step in order for this argument to apply.

It is respectfully noted that claim 4 is not rejected under 35 U.S.C. § 112, second paragraph, therefore, Applicants' arguments regarding the missing interrelations between the steps are moot.

Applicants further argued that:

MPEP § 2172.01 only authorizes a rejection when the "the specification or [ ] other statements of record" state the certain elements are "essential." Personal judgment is not a permissible basis to determine that an element is "essential." The Office Action points to no statements in the "specification or in other statements of record" to establish that any element is "essential." The Office Action is too incomplete to raise any rejection."

While The Office recognizes that "[a] claim which omits matter disclosed to be essential to the invention as described in the specification or in other statement of record may be rejected under 35 U.S.C. § 112, first paragraph, as not enabling[,]" the Office nonetheless respectfully notes that, first, the Office action does not specifically make a rejection of claim 2 or claim 4 under 35 U.S.C. § 112, first paragraph as not enabling; and second, "disclosed to be essential," shown in MPEP § 2172.01, does not necessarily mean that the disclosure or any statements of record has to specifically states that "[this step] is essential to the invention." For the sake of argument, even assuming that the Office made a rejection of claim 2 under 35 U.S.C. § 112, first paragraph as not enabling, the Office's interpretation of the statement "disclosed to be essential" is that without the step recited in claim 4, the invention claimed in claim 2 would be operative independently then the step in claim 4 will be not an essential step. In this instance, without "the stream of instructions" resulted from the translation of at least a segment of binary representation of a program, without the "annotating in the produced instructions memory loads" etc., as recited in claim 4, would the invention claimed in claim 2 be operative? In the answer to this

question is no, then the steps recited in claim 4 are essential to the invention without the requirement that these steps be stated "to be essential" in the specification. Any one of ordinary skill in the art would reach the same conclusion after interpreting the claims in light of the specification. Therefore, this is not personal judgment.

The Office would appreciate a statement from Applicants that the invention claimed in claim 2 is indeed operative without the step and/or features recited in claim 4 and the steps and/or features in claim 4 are not essential to the practice of the invention recited in claim 2.

Applicants further argued that "[t]he Office action states a different rationale, not authorized by MPEP § 2172.01. The rationale stated in the Office action was abolished fifty years ago..." See Applicants' Remarks, page 9, 2nd, 3rd and 4th ¶¶s. In response, the Office respectfully directs Applicants' attention to Form Paragraphs 7.30.02 and 7.34.13 in the MPEP which have been used by the Office. If this rationale has been abolished fifty years ago, then the Office should be advised to revise these form paragraphs.

Applicants also argued that "[t]he purpose of claims is not to explain the technology or how it works, but to state the legal boundaries of the patent grant."

In response, it is not known clearly what the legal boundaries of claim 2 and 14 are, as previously discussed in the response to Applicants' first two arguments of paragraph V.

VI. Paragraphs 16-19: Claims 2 and 14 Recite § 101 Patentable Subject Matter

In response to Applicants' arguments at page 10 of their Remarks, the Office respectfully notes that not only claim 2 does not recite any transformation of data because claim 2 only claims a sole evaluating which does not produce any useful, concrete and tangible result. See Interim Guidelines for Examination of patent Applications for Patent Subject Matter Eligibility, IV.C.2.

In response to Applicants' argument that the Office action misquotes the cases and MPEP section it relies on, the Office notes that as concurred by Applicants that MPEP § 2106(IV)(B)(1)(a) a program or data structure might require a computer-readable medium. The Office also notes that claim 14 recites a computer comprising instruction execution circuitry designed to evaluate the condition recited in the claim. As best understood by the Office and discussed in the Office action in paragraphs 18 and 19, the claim is only directed to a computer comprising a circuit designed to perform a function. There is no program or instruction code stored on a computer-readable medium to permits the claimed to be realized.

Furthermore, as discussed in paragraph 18 of the Office action, without a program or instruction code instructing the computer to perform these instructions to permit the claimed function to be realized the claimed invention is inoperative and lacks utility.

VII. Conclusion

In view of the foregoing discussion, the rejection of claims 2, 9, 10, 12-14, 19-22 and 30 is considered proper and maintained.

Claim Rejections – 35 USC §112

5. The following is a quotation of the first paragraph of 35 U.S.C. §112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claim 14 is rejected under 35 U.S.C. § 112, first paragraph, as being single means claim. MPEP 2164.08(a).

A single means claim, i.e., where a means recitation does not appear in combination with another recited element of means, is subject to an undue breath rejection under 35 U.S.C. § 112, first paragraph. ***In re Hyatt***, 708 F 2.d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983) (A single means claim which covered every conceivable means for achieving the stated purpose was held nonenabling for the scope of the claim because the specification disclosed at most only those means known to the inventor.). When claims depend on a recited property, a fact situation comparable to ***Hyatt*** is possible, where the claims cover every conceivable structure (means) for achieving the stated property (result) while the specification discloses at most only those known to the inventor.

In the instant application, Claim 14 covers every conceivable structure (e.g., instruction execution circuitry) for achieving the stated purpose of evaluating, based at least in part on an annotation encoded in a segment descriptor, whether an individual memory-reference instruction (or an individual memory reference of an instruction), references a device with a valid memory address that cannot be guaranteed to be well-behaved while the specification discloses at most only those known to the inventor.

Furthermore, it should be noted that although Claim 14 is interpreted in light of the specification, the limitations of the instruction execution circuitry described in the specification will not be read into Claim 14. Accordingly, any arguments that the

limitations described in the specification provide patentable distinction over the prior art will be unpersuasive.

7. The following is a quotation of the second paragraph of the 35 U.S.C. § 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 2 is rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: producing a stream of instructions, generating memory references, determining whether or not memory addresses are guaranteed to be well-behaved, annotating in the instructions the results of the determining step, encoding and storing the annotation in a segment descriptor. These omitted steps are considered critical and essential because without the pre-performance of these steps, the claimed single step of evaluating is not operative. Alternatively stated, it is unclear as to how the evaluating step could be performed without the existence of a stream of instructions, the execution of which generates memory references, the existence of annotation stored in a segment descriptor that indicates whether or not the address where a device is located in the memory system is an address that cannot be guaranteed to be well-behaved.

9. Claim 14 is rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are at least: a device, a storage medium, a binary translator software and a circuitry to raise an exception. The existence and thus the claim of a device that is associated with the instruction execution circuitry are considered essential and critical for the instruction

execution circuitry to be able to reference. The existence and thus the claim of a storage medium are essential and critical to provide the device with a storage area having an address. The existence and thus the claim of a binary translator software are essential and critical in order to generate the memory-reference instruction, provide a segment descriptor to encode an annotation and to give an indication whether or not the memory address of the device is valid and guaranteed to well-behaved. A claim to a circuitry without the above-mentioned elements software is considered incomplete, non-enabling and devoid of any utility.

Double Patenting

10. The non-statutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper time wise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ 2d 2010 (Fed. Cir. 1993); *In re Long*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1993); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Voge*, 422 F2.d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F2.d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.103(c) 1.321(c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.37(b).

11. Claims 2+3 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 4+7 of '379 Patent in view of U.S. Patent No. 5,926,484 to Takusagawa.

Instant Claims 2+3	Patent/Copending Claims 4+7
2. A method, comprising the step of:	
for memory references generated as part of executing a stream of instructions on a computer, evaluating whether an individual memory reference of an instruction references a device having a valid memory address but that cannot be guaranteed to be well-behaved, based at least in part on an annotation encoded in a segment descriptor.	
	issuing a successful memory reference from a computer CPU to a bus;
	recording in a storage of the computer whether a device accessed over the bus by the memory reference is well-behaved memory or not well-behaved memory
3. A method of claim 2, further comprising the step of:	7. The method of claim 4, further comprising the steps of:
if the reference cannot be guaranteed	evaluating whether an individual

to be well-behaved, re-executing the instruction in an alternative execution mode.	memory reference of an instruction references a device that cannot be guaranteed to be well-behaved, and if the reference cannot be guaranteed to be well-behaved, re-executing the instruction in an alternative execution mode.

A question of patentability is raised with respect to representative Claims 2+3 of the instant application under the judicially created doctrine of "obviousness-type" double patenting with respect to '379 Patent Claims 4+7 (note that Applicants' argument – page 2 – incorrectly refers to '379 Patent Claims 4+78) in view of U.S. Patent No. 5,926,484 to Takusagawa.

Takusagawa discloses a device having a valid memory address (see at least Claim 9, first address register storing a valid address), issuing a successful memory reference from a computer CPU to a bus (see at least Claim 8, first stage for receiving a request issued by a processor for accessing a memory) and recording in a storage of the computer whether a device accessed over the bus by the memory reference is well-behaved memory or not well-behaved memory (see at least Claim 12, resetting first valid register to an invalid state – i.e., *recording in a storage of the computer* – when no fault is detected, i.e., *well-behaved memory* and resetting a third valid register to an invalid state and setting a pending register to a pending state when a fault is detected, i.e., *not well-behaved memory*).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to add the above steps taught by Takusagawa to the '379 Patent teachings as this would provide the '379 Patent teachings with necessary

information to determine whether a memory is well-behaved or not well-behaved for the purpose of making appropriate corrections to improve system reliability and performance as suggested by Takusagawa (1:39-42).

12. A question of patentability is raised with respect to Claim 22 of the instant application under the judicially created doctrine of "obviousness-type" double patenting with respect to '379 Patent Claims 4+8 in view of U.S. Patent No. 5,926,484 to Takusagawa.

'379 Patent Claims 4+8 contain every element of instant Claim 22 (i.e., **anticipate** Claim 22) except the limitation *based at least in part on an annotation encoded in a segment descriptor, and aborting the identified memory load* and *based at least in part on the identifying* (it should be noted that although '379 Patent Claims 4+8 contain the additional steps (e.g., of issuing and of recording) as pointed out by Applicants, an important issue that needs to be considered is that Patent Claims 4+8 **anticipate** every limitation of Instant Claim 22, except the above-mentioned limitations).

However, Takusagawa discloses the limitations *based at least in part on an annotation* and *on the identifying*. See at least 2:40-43 and discussion hereinafter in conjunction with the rejection of Claims 2 and 14 under 35 U.S.C. § 102 (a) as being anticipated by Takusagawa. The limitation *aborting the identified memory load* is also disclosed by Takusagawa in the Abstract, lines 6-7, e.g., "the processing of the request is suppressed by a pending register," and related text in the specification.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to add the above steps taught by Takusagawa to the '379 Patent teachings as this would provide the '379 Patent teachings with necessary information to determine whether a memory is well-behaved or not well-behaved for the purpose of making appropriate corrections to improve system reliability and performance as suggested by Takusagawa (1:39-42).

13. A question of patentability is raised with respect to Claim 30 of the instant application under the judicially created doctrine of "obviousness-type" double patenting with respect to '379 Patent Claims 4+8 in view of U.S. Patent No. 5,926,484 to Takusagawa.

'379 Patent Claims 4+8 contain every element of instant Claim 30 (i.e., **anticipate** Claim 30) except the limitation *instruction execution circuitry* and *based at least in part on an annotation encoded in a segment descriptor* (it should be noted that although '379 Patent Claims 4+8 contain the additional steps (e.g., of issuing and of recording) as pointed out by Applicants, an important issue that needs to be considered is that Patent Claims 4+8 **anticipate** every limitation of Instant Claim 30, except the above-mentioned limitations).

However, Takusagawa discloses the limitations *based at least in part on an annotation.* See at least 2:40-43 and discussion hereinafter in conjunction with the rejection of Claims 2 and 14 under 35 U.S.C. § 102 (a) as being anticipated by Takusagawa. The limitation *instruction execution circuitry* is also disclosed by Takusagawa in FIG. 1 and related text.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to add the above features taught by Takusagawa to the '379 Patent teachings as this would provide the '379 Patent teachings with necessary information and circuitry to determine whether a memory is well-behaved or not well-behaved for the purpose of making appropriate corrections to improve system reliability and performance as suggested by Takusagawa (1:39-42).

Claim Rejections – 35 USC § 101

14. 35 U.S.C. § 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the condition and requirements of this title.

15. Claims 2, 10 and 13 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

Under the most recent Federal Circuit cases, transformation of data by a machine (e.g., a computer) is statutory subject matter provided the claims recite "practical application, i.e., 'a useful, concrete and tangible result.'" State St Bank & Trust Co. v. Signature Fin. Group, Inc., 149 F.3d 1368, 1373, 47 USPQ 2d 1596, 1600-01 (Fed. Cir. 1998).

In this instant application, the language of Claim 2 raises a question as to whether this claim is merely directed to an abstract idea that is not tied to a machine which would result in a practical application producing a concrete, useful, and tangible result to form the basis for a statutory subject matter under 35 U.S.C. § 101.

The Office's interpretation of Claim 2 is that this claim does not expressly or implicitly recite any **transformation** of data by a machine. Structure will not be read into the claims for the purposes of the statutory subject matter analysis although the steps might be capable of being performed by a machine.

The single step of evaluating whether an individual memory reference of an instruction references a device having a valid address... based at least in part on an annotation encoded in a segment descriptor does not expressly or implicitly indicate any **transformation of** any **data**. Furthermore, this step does not specifically or implicitly require performance of the step by a machine

in order to produce useful, concrete and tangible results as formulated in State Street case law.

Claims 10 and 13, which depend from Claim 2, are also rejected under 35 U.S.C. § 101 for the same reasons.

16. Claim 14 is rejected under 35 U.S.C. § 101 because the claimed invention is inoperative and therefore lacks utility.

Claim 14 recites a computer comprising instruction execution circuitry **designed** to evaluate, based at least in part on an annotation encoded in a segment descriptor, whether an individual memory-reference instruction ... references a device with a valid memory address... The Office's interpretation of Claim 14 is that this claim only recites an instruction execution circuitry **designed** to evaluate a certain instruction. Claim 14 does not expressly or implicitly require the instruction execution circuitry to actually perform the act of evaluating since the language of the claim only indicates that the circuitry is **designed** to perform the evaluation. Without any act being performed, the claimed invention lacks utility.

17. Claim 14 is rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

A claim that recites a computer without a computer program encoded on a computer-readable medium to instruct the computer to perform a certain process does not define structural and functional interrelationships between the computer (which permits the computer program's functionality to be realized) and the computer program and is thus not statutory. *Warmerdam*, 33 F.2d at 1361, 31 USPQ 2d at 1760. *In re Sarkar*, 588 F.2d 1330, 1333, 200 USPQ 132, 137 (CCPA 178). See MPEP §2106 (IV)(B)(1)(a).

Claims 19-21, which depend from Claim 14, are also rejected under 35

U.S.C. § 101 for the same reasons.

Claim Rejections – 35 USC § 102

18. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejection under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or foreign country, before the invention thereof by the applicant for patent.

19. Claims 2, 9, 12 and 14 are rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 5,926,484 to Takusagawa.

Claim 2

Takusagawa discloses at least a method, comprising the step of (see at least FIG. 1 in conjunction with FIG. 5 and related text):

> *for memory references generated as part of executing a stream of instructions on a computer* (see at least 4:36-38), *evaluating* (see at least 2:50-62) *whether an individual memory reference of an instruction* (4:36-38; wherein the *individual memory reference of an instruction* is interpreted to mean address of the request) *references a device having a valid memory address but that cannot be guaranteed to be well-behaved, based at least in part on an annotation encoded in a segment descriptor* (see at least 2:40-43; *valid memory address* is indicated by a 1 in the valid field, *cannot be guaranteed to be well-behaved* is indicated by 0 in the clean field).

Claim 9

The rejection of base claim 1 is incorporated. Takusagawa further

discloses *wherein the device having a valid memory address has an address in an I/O space of the computer* (see at least FIG. 1, e.g., the store-in cache memory).

Claim 12

The rejection of base claim 1 is incorporated. Takusagawa further discloses *wherein the segment descriptor is stored in a segment register* (see at least FIG. 1, e.g., the valid register).

Claim 14

Since Claim 14 recites a computer that performs the same method step of Claim 2, the same rationale set forth in the rejection of Claim 2 also applies to the rejection of Claim 14.

Allowable Subject Matter

20. Claims 3-8, 10-11, 13, 15-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

21. Claims 1, 40-54, 55-59 and 61-65 are allowed.

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoang-Vu "Antony" Nguyen-Ba whose telephone number is (571) 272-3701. The examiner can normally be reached on the following days of a bi-week: Monday-Thursday (first week) and Tuesday-Friday (second week) from 7:45 am to 6:15 pm.

If attempts to reach the examiner are unsuccessful, the examiner's supervisor, Tuan Dam can be reached at (571) 272-3695.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

ANTONY NGUYEN-BA
PRIMARY EXAMINER

July 7, 2006